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Application No.: filed concurrently  
October 19, 2005

IN THE CLAIMS

Please substitute the following claims for the pending claims with the same numbers respectively:

Claim 1 (Original): A semiconductor memory card used by being connected to an access unit, comprising:

a host interface section which sends a control signal and data to said access unit and receives a signal from said access unit;

a nonvolatile memory which includes a plurality of nonvolatile memory chips and in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing;

a memory controller which controls erasing, writing, and reading of data with respect to said nonvolatile memory; and

a host information memory which temporarily stores a data write start address and a data size value given by said access unit, wherein

said memory controller includes a free physical area generation section which determines whether or not to perform erasing of invalid blocks of said nonvolatile memory based on the

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data write start address and the data size value temporarily stored in said host information memory, and simultaneously performs writing of data to one nonvolatile memory chip and erasing of blocks of another nonvolatile memory chip when performing erasing of said invalid blocks.

Claim 2 (Original): The semiconductor memory card according to claim 1, wherein said free physical area generation section determines the number of blocks to be erased so that an erase time corresponds to a write time of write data.

Claim 3 (Original): The semiconductor memory card according to claim 1, wherein said memory controller is connected to each of said plurality of nonvolatile memory chips with respectively independent bidirectional buses.

Claim 4 (Original): The semiconductor memory card according to claim 1, wherein said nonvolatile memory is composed of two nonvolatile memory chips in which, while a write process is performed in one nonvolatile memory chip, erasing of invalid blocks is performed in the other nonvolatile memory chip.

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Claim 5 (Original): A semiconductor memory control apparatus used by being connected to a nonvolatile memory which includes a plurality of nonvolatile memory chips and in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing:

a host interface section which sends a control signal and data to an access unit and receives a signal from said access unit;

a memory controller which controls erasing, writing, and reading of data with respect to said nonvolatile memory; and

a host information memory which temporarily stores a data write start address and a data size value given by said access unit, wherein

said memory controller includes a free physical area generation section which determines whether or not to perform erasing of invalid blocks of said nonvolatile memory based on the data write start address and the data size value temporarily stored in said host information memory, and simultaneously performs writing of data to one nonvolatile memory chip and erasing of blocks of another nonvolatile memory chip when performing erasing of said invalid blocks.

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Claim 6 (Original): The semiconductor memory control apparatus according to claim 5, wherein said free physical area generation section determines the number of blocks to be erased so that an erase time corresponds to a write time of write data.

Claim 7 (Original): The semiconductor memory control apparatus according to claim 5, wherein said memory controller is connected to each of said plurality of nonvolatile memory chips with respectively independent bidirectional buses.

Claim 8 (Original): The semiconductor memory control apparatus according to claim 5, wherein said nonvolatile memory is composed of two nonvolatile memory chips in which, while a write process is performed in one nonvolatile memory chip, erasing of invalid blocks is performed in the other nonvolatile memory chip.

Claim 9 (Original): A semiconductor memory control method in a semiconductor memory card having a nonvolatile memory which includes a plurality of nonvolatile memory chips and in which a plurality of continuous sectors is grouped to be a block as a

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minimum unit of data erasing, said semiconductor memory control method comprising the steps of:

temporarily storing a data write start address and a data size value given by an access unit in a host information memory;

determining whether or not to perform erasing of invalid blocks of said nonvolatile memory based on the data write start address and the data size value temporarily stored in said host information memory; and

simultaneously performing writing of data to one nonvolatile memory chip and erasing of blocks of another nonvolatile memory chip when performing erasing of said invalid blocks.

Claim 10 (Original): The semiconductor memory control method according to claim 9, further comprising the step of determining the number of blocks to be erase so that an erase time corresponds to a write time of write data when erasing of invalid blocks of said nonvolatile memory is performed.

Claim 11 (Original): The semiconductor memory control method according to claim 9, said nonvolatile memory is composed of two nonvolatile memory chips in which, while a write process

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is performed in one nonvolatile memory chip, erasing of an invalid block is performed in the other nonvolatile memory chip.

Please add new claims 12-24 as follows.

Claim 12 (New): A semiconductor memory card used by being connected to an access unit, comprising:

a host interface section which sends a control signal and data to said access unit and receives a signal from said access unit;

a nonvolatile memory which includes a plurality of nonvolatile memory chips and in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing;

a memory controller which is connected to each of said plurality of nonvolatile memory chips with respectively independent bidirectional buses and controls erasing, writing, and reading of data; and

a host information memory which temporarily stores a write speed mode given by said access unit, wherein

said memory controller includes a nonvolatile memory access section which performs writing with respect to said plurality of

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nonvolatile memory chips with controlling write timing to each of said plurality of nonvolatile memories depending on a speed mode stored in said host information memory.

Claim 13 (New): The semiconductor memory card according to claim 12, wherein said memory controller performs, in parallel, writing with respect to said plurality of nonvolatile memory chips when the write speed mode stored in said host information memory is a high speed mode, and sequentially performs writing with respect to said plurality of nonvolatile memory chips when the write speed mode stored in said host information memory is a low speed mode.

Claim 14 (New): A semiconductor memory control apparatus used by being connected to a nonvolatile memory which includes a plurality of nonvolatile memory chips in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing:

a host interface section which sends a control signal and data to an access unit and receives a signal from said access unit;

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a memory controller which is connected to each of said plurality of nonvolatile memory chips with respectively independent bidirectional buses and controls erasing, writing, and reading of data; and

a host information memory which temporarily stores a write speed mode given by said access unit, wherein

said memory controller includes a nonvolatile memory access section which performs writing with respect to said plurality of nonvolatile memory chips with controlling write timing to each of said plurality of nonvolatile memories depending on the speed mode stored in said host information memory.

Claim 15 (New): The semiconductor memory control apparatus according to claim 14, wherein said memory controller performs, in parallel, writing with respect to said plurality of nonvolatile memory chips when the write speed mode stored in said host information memory is a high speed mode, and sequentially performs writing with respect to said plurality of nonvolatile memory chips when the write speed mode stored in said host information memory is at a low speed mode.

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Claim 16 (New): A semiconductor memory control method in a semiconductor memory card having a nonvolatile memory which includes a plurality of nonvolatile memory chips and in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing and a host information memory for temporarily storing a write speed mode given by an access unit, said semiconductor memory control method comprising the step of:

performing writing with respect to said plurality of nonvolatile memory chips with controlling write timing to each of said plurality of nonvolatile memories depending on the speed mode stored in said host information memory.

Claim 17 (New): The semiconductor memory control method according to claim 16, further comprising the steps of:

performing, in parallel, writing with respect to said plurality of nonvolatile memory chips when the write speed mode stored in said host information memory is a high speed mode, and sequentially performing writing with respect to said plurality of nonvolatile memory chips when the write speed mode stored in said host information memory is a low speed mode.

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Claim 18 (New): A semiconductor memory card used by being connected to an access unit, comprising:

a host interface section which sends a control signal and data to said access unit and receives a signal from said access unit;

a nonvolatile memory which includes a plurality of nonvolatile memory chips and in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing;

a memory controller which controls erasing, writing, and reading of data with respect to said nonvolatile memory; and

a host information memory which temporarily stores a defragmentation instruction signal given by said access unit, wherein

said memory controller includes a free physical area generation section which detects a remaining amount of erased blocks of said nonvolatile memory, issues a defragmentation request signal to said access unit when the number of erased blocks is a predetermined number or less, and executes defragmentation when the defragmentation instruction signal is temporarily stored in said host information memory.

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Claim 19 (New): A semiconductor memory control apparatus used by being connected to a nonvolatile memory which includes a plurality of nonvolatile memory chips and in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing, said semiconductor memory control apparatus comprising:

a host interface section which sends a control signal and data to an access unit and receives a signal from said access unit;

a memory controller which controls erasing, writing, and reading of data with respect to said nonvolatile memory; and

a host information memory which temporarily stores a defragmentation instruction signal given by said access unit, wherein

said memory controller includes a free physical area generation section which detects a remaining amount of erased blocks of said nonvolatile memory, issues a defragmentation request signal to said access unit when the number of erased blocks is a predetermined number or less, and executes defragmentation when the defragmentation instruction signal is temporarily stored in said host information memory.

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Claim 20 (New): A semiconductor memory control method in a semiconductor memory card having a nonvolatile memory which includes a plurality of nonvolatile memory chips and in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing, said semiconductor memory control method comprising the steps of:

temporarily storing a defragmentation instruction signal given by an access unit in a host information memory;

detecting a remaining amount of erased blocks of said nonvolatile memory;

issuing a defragmentation request signal to said access unit when the number of erased blocks is a predetermined number or less; and

executing defragmentation when the defragmentation instruction signal is temporarily stored in said host information memory.

Claim 21 (New): A semiconductor memory card used by being connected to an access unit, comprising:

a host interface section which sends a control signal and data to said access unit and receives a signal from said access unit;

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a nonvolatile memory in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing, and in which an address management information area and a user data area are stored in respective different blocks;

a memory controller which has a volatile memory holding address management information, performs erasing, writing, and reading of data, and updates said volatile memory in every erasing, and writing of data; and

a host information memory which temporarily stores an address management information update signal transferred from said access unit, wherein

said memory controller includes a nonvolatile memory access section which writes data transferred when a write command and data are given by said access unit to said nonvolatile memory, erases blocks designated when an erase command is given, and writes address management information held in the volatile memory of said memory controller to the address management information area of said nonvolatile memory when said address management information update signal is held in said host information memory.

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Claim 22 (New): A semiconductor memory control apparatus used by being connected to a nonvolatile memory in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing, and in which an address management information area and a user data area are stored in respective different blocks, said semiconductor memory control apparatus comprising:

a host interface section which sends a control signal and data to an access unit and receives a signal from said access unit;

a memory controller which has a volatile memory holding address management information, performs erasing, writing, and reading of data with respect to said nonvolatile memory, and updates said volatile memory in every erasing, and writing of data; and

a host information memory which temporarily stores address management information update signal transferred from said access unit, wherein

said memory controller includes a nonvolatile memory access section which writes data transferred when a write command and data are given by said access unit to said nonvolatile memory, erases blocks designated when an erase command is given, and

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writes address management information held in the volatile memory of said memory controller to the address management information area of said nonvolatile memory when said address management information update signal is held in said host information memory.

Claim 23 (New): A semiconductor memory control method in a semiconductor memory card having a nonvolatile memory in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing, and in which an address management information area and a user data area are stored in respective different blocks, said semiconductor memory control method comprising the steps of:

updating a volatile memory, which is provided for holding address management information, in every erasing, and writing of data with respect to said nonvolatile memory;

temporarily storing an address management information update signal transferred from said access unit in a host information memory;

writing data transferred when a write command and data are given by said access unit to said nonvolatile memory;

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erasing blocks designated when an erase command is given;  
and

writing the address management information held in said  
volatile memory to the address management information area of  
said nonvolatile memory when said address management information  
update signal is held in said host information memory.